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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
|-----------------|-------------|----------------------|---------------------|------------------|

10/780,317

02/17/2004

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5367-69

9751

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03/17/2006

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EXAMINER

NOVACEK, CHRISTY L


ART UNIT

PAPER NUMBER

2822

DATE MAILED: 03/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | | |
|------------------------------|--------------------------------|---|--|
| Office Action Summary | Application No. 10/780,317 | Applicant(s) HARLE ET AL.  | |
| | Examiner Christy L. Novacek | Art Unit 2822 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 January 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This office action is in response to the amendment filed January 3, 2006.

Response to Amendment

The amendment of claims 3, 4, 6, 7 and 14 is sufficient to overcome the objections to claims 3, 4, 6, 7, 14 and 15 stated in the previous office action. Therefore, these objections are withdrawn.

The amendment of claims 16, 18, 20 and 21 is sufficient to overcome the rejections of claims 16, 18, 20 and 21 under 35 U.S.C. 112, second paragraph stated in the previous office action. Therefore, these rejections are withdrawn.

Claim Rejections - 35 USC § 102

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1, 4 and 6-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Koike et al. (EP 1263031, cited in IDS).

Regarding claim 1, Koike discloses forming a mask layer (4) over a substrate (1) or over an initial layer (20), such that the mask layer has a plurality of windows leading to the substrate or to the initial layer. A semiconductor material (32) that is to be grown onto the substrate in a subsequent method step substantially cannot be grown or can be grown to a significantly reduced extent onto the mask layer by comparison with the substrate or the initial layer. The substrate or the initial layer is etched back in the windows, in such a manner that pits are formed in the substrate or in the initial layer starting from these windows. Semiconductor material is grown

Art Unit: 2822

onto the substrate or onto the initial layer, in such a manner that lateral growth is promoted and the semiconductor material initially grows primarily from the flanks of the pits toward the center of the pits where they form a coalescence region, so that defects in the substrate or in the initial layer which impinge on the flanks of the pits bend off toward the center of the pits in the semiconductor material, and then, starting from the windows, grows over the mask layer and in each case grows together over the mask layer between adjacent windows, where it forms a further coalescence region. A component layer sequence (104/105/106/107/108/109) is grown onto the semiconductor material (Fig. 1-2; para. 0030).

Regarding claim 4, Koike discloses that a cross section of the pits perpendicular to the plane of the substrate can be formed in a V shape (para. 0037).

Regarding claim 6, Koike discloses that the semiconductor material (32) is grown using an epitaxial lateral overgrowth (ELOG) technique (para. 0002).

Regarding claims 7 and 20, Koike discloses that the grown semiconductor material (32) has a substantially planar surface (Fig. 1E).

Regarding claim 8, Koike discloses that the mask layer can have a lattice-like or mesh-like structure (Fig. 10A).

Regarding claim 9, Koike discloses that the mask layer may be made of silicon nitride (para. 0042).

Regarding claim 10, Koike discloses that the semiconductor material (32) and/or the component layer sequence includes a compound of elements from the main groups III and V (para. 0002, 0052).

Art Unit: 2822

Regarding claim 11, Koike discloses that the semiconductor material (32) and/or the component layer sequence includes a nitride compound semiconductor material (para. 0002, 0052).

Regarding claim 12, Koike discloses that the semiconductor material (32) can include a composition selected from the system $\text{In}_x\text{Al}_y\text{Ga}_{1-x-y}\text{N}$, where $0 \leq x \leq 1$, $0 \leq y \leq 1$ and $x+y \leq 1$ (para. 0002).

Regarding claim 13, Koike discloses that the substrate can be made of silicon, silicon carbide, or sapphire (para. 0032).

Regarding claim 14, Koike discloses forming an electronic semiconductor body (para. 0051-0065) according to the steps recited above in reference to claim 1.

Regarding claim 15, Koike discloses that the electronic semiconductor body is a radiation-emitting semiconductor chip, in particular a light-emitting diode chip or a laser diode chip (para. 0051-0065).

Regarding claims 16 and 18, Koike discloses that the plurality of semiconductor bodies are made of nitride compound semiconductor material.

Regarding claim 17, Koike discloses forming a mask layer (4) over an underlying layer (31), wherein the mask layer has a plurality of windows over the underlying layer, and wherein the underlying layer includes at least one of a substrate and an initial layer. Koike discloses etching, through the windows in the mask layer, pits in the underlying layer. Koike discloses depositing a semiconductor material (32) by growing the semiconductor material laterally from flanks of the pits in the underlying layer, wherein first coalescence regions are formed substantially in the center of each of the pits, wherein defects in the underlying layer which

Art Unit: 2822

contact the sides of the pits propagate in said semiconductor material in a lateral direction toward the first coalescence regions, and growing the semiconductor material outward from the windows, as the windows become full of deposited semiconductor material, over the mask layer, wherein second coalescence regions are formed above the mask layer (Fig. 1-2; para. 0030).

Regarding claim 19, Koike discloses forming a layer of the semiconductor material above both the mask layer and the pitted underlying layer (Fig. 1E).

Regarding claim 21, Koike discloses growing a sequence of component layers (104/105/106/107/108/109) on the substantially planar semiconductor material surface (Fig. 2).

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koike (EP 1263031, cited in IDS) in view of Hageman et al. ("Improvement of the Optical and Structural Properties of MOCVD Grown GaN on Sapphire by an in-situ SiN Treatment", cited in IDS).

Regarding claim 2, Koike discloses that the growth of the semiconductor material is effected by means of metalorganic vapor phase epitaxy (para. 0033). Koike does not disclose all the specifics of the epitaxial process, neither does Koike disclose how the mask layer is formed on the underlying layer. Like Koike, Hageman discloses forming a mask layer of SiN over a substrate and then using MOCVD to epitaxially grow a Group III nitride compound over the mask layer (pg. 660). Hageman discloses in-situ depositing the SiN mask material on the substrate in an epitaxy reactor in such a manner that a discontinuous mask layer is formed, in

Art Unit: 2822

which windows leading to the substrate are already formed during the deposition of the mask layer (pg. 660). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Hageman to form the SiN mask layer of Koike because Koike does not disclose any particular method of forming the mask layer and Hageman teaches a method of forming the mask layer that results in a stable SiN mask that allows epitaxial growth of a Group III nitride compound layer that has improved optical and structural properties.

Regarding claim 3, Koike discloses depositing the initial layer epitaxially, but does not specifically disclose depositing the initial layer in-situ in the epitaxial reactor. At the time of the invention, it would have been obvious to one of ordinary skill in the art to deposit the initial layer in-situ in the epitaxial reactor because by depositing the initial layer in-situ, the substrate can be protected from contamination which would result from transporting the substrate out of the reactor between deposition steps and because, by depositing the initial layer in-situ, fewer process steps are required and the method of Koike can thereby be carried out more efficiently.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Koike (EP 1263031, cited in IDS).

Regarding claim 5, Koike does not specifically disclose that the semiconductor material (32) includes a plurality of layers of different compositions. However, Koike discloses forming a plurality of layers of different compositions over the semiconductor material. At the time of the invention, it would have been obvious to one of ordinary skill in the art to deposit the plurality of overlying layer of Koike of the same epitaxial growth process used to grow the semiconductor material (32) because Koike does not teach any particular method of depositing these plurality of overlying layers and because by depositing the plurality of overlying layers

Art Unit: 2822

epitaxially in-situ, the substrate can be protected from contamination which would result from transporting the substrate out of the reactor between deposition steps and because, by depositing the plurality of overlying layers in-situ, fewer process steps are required and the method of Koike can thereby be carried out more efficiently.

Response to Arguments

Applicant's arguments filed January 3, 2006 have been fully considered but they are not persuasive.

Regarding the rejections of claims 1 and 17 as being anticipated by Koike, Applicant argues that Koike allegedly discloses forming the trenches in the semiconductor layer 31, whereas Applicant discloses forming the trenches in the substrate. However, claims 1 and 17 do not recite that the trenches (pits) must be etched into the substrate. Claim 1 recites, "etching back the substrate (1) **or the initial layer (2)** in the windows (4), in such a manner that pits (41) are formed in the substrate (1) **or in the initial layer (2)**" (emphasis added). Claim 17 recites, "said underlayer comprises at least one of a substrate and an initial layer" and "etching, through the windows in the mask layer, pits in the underlying layer". Therefore, claims 1 and 17 recite that the pits can be formed in either the substrate or in the initial layer. As discussed above, the layer 20 taught by Koike is considered to equate to "the initial layer (2)" recited in claims 1 and 17. Figures 6A-6D show forming trenches (pits) in the layer 20. Therefore, Koike meets the limitations of claims 1 and 17. Additionally, it is noted that column 10, lines 40-49 of Koike states, "The above-described Group III nitride compound semiconductor having regions where threading dislocation is suppressed can be formed as a Group III nitride compound

Art Unit: 2822

semiconductor substrate through removal of, for example, the substrate 1, the buffer layer 2, and portions of the Group III nitride compound semiconductor where threading dislocation is not suppressed. The thus-formed substrate allows formation of a Group III nitride compound semiconductor device thereon or may be used as a substrate for forming a greater Group III nitride compound semiconductor crystal.” In other words, the layer 20 may itself serve as a substrate.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

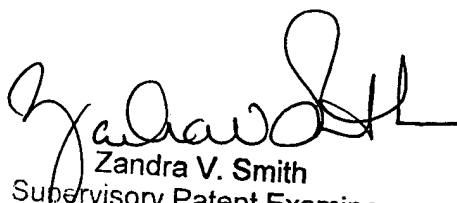
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

Art Unit: 2822

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLN
March 14, 2006


Zandra V. Smith
Supervisory Patent Examiner
March 18, 2006